Improving the Power-Added Efficiency of FET Amplifiers Operating with Varying-Envelope Signals

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Abstract—A technique is proposed for improving the power-added efficiency of linear, class-A FET power amplifiers operating with varying-envelope signals. It involves dynamically controlling the gate "dc" bias voltage with the envelope of the input RF signal. It is shown theoretically that this technique, which is referred to as "class Ã," results in a significant improvement in the power-added efficiency over standard class A, independently of the FET power gain. The efficiency is also better than that of standard class B if the FET gain is less than about 10 dB, which is the case normally encountered at higher microwave frequencies. The practical implementation of class Ã requires FET's with essentially linear drain-current-versus-gate-voltage transfer characteristics.

I. Introduction

THE MODULATION and multiplexing schemes used in many communication systems result in signals having highly time-varying envelopes. This is the case, for example, in frequency-division-multiplex systems employing either multiple carriers or single-sideband (SSB) signals, and in bandwidth-efficient digital systems employing quadrature amplitude modulation (QAM). A power amplifier employed in any of these systems is required to operate with a reasonable degree of linearity. This is accomplished by backing off the average output power of the amplifier away from saturation so as to restrict the range of signal envelope variations to the essentially linear region of amplification. In class-A field-effect-transistor (FET) power amplifiers, the dc bias power is basically independent of the signal level. Thus the amplifier efficiency is reduced from its peak (saturation) value by the amount of backoff. Such a reduction in efficiency results in a severe power penalty which could be unacceptable, especially on a satellite where the dc power is quite costly.

A proposed technique for improving the efficiency of class-A FET power amplifiers operating with varying-envelope signals is depicted in Fig. 1. It will be referred to as "class Ã." The envelope of a sample of the input RF signal is detected, and is used to dynamically control the gate "dc" bias voltage $E_G(t)$. This is done such that the drain "dc" bias current $I_D(t)$ is forced to be proportional to the signal envelope. This current is not a direct current in the formal sense; rather, it is the sum of a constant component $\bar{I}_D$ and a fluctuating component that varies at the envelope rate. A large capacitance C is included in the drain bias circuit to bypass the latter component of current

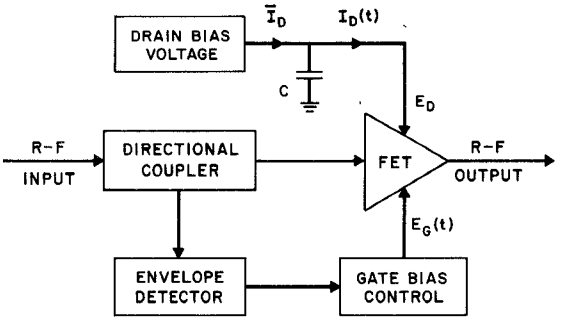

Fig 1 The proposed class-Ã mode of operation for improving the efficiency of FET power amplifiers operating with varying-envelope signals.

while maintaining an almost constant drain bias voltage E_D. Note that the gate control circuit should consume a negligible amount of power since the gate draws practically no dc current.

Linear operation of an FET power amplifier in class Ã requires nearly constant gain over a large range of gate bias voltage. This requires the FET to have an essentially linear drain-current-versus-gate-voltage transfer characteristic. This characteristic can be obtained through the use of specially shaped channel-doping profiles [1]–[4]. It is to be noted that the linear operation of a standard class-A amplifier, over a frequency range of less than an octave, is possible even if the transfer characteristic contains a quadratic term. In fact, many FET's available in practice are of that type since it is less restrictive on the required shape of the channel-doping profile [5], [6].

The statistics of several important types of varying-envelope signals are studied in Section II. An idealized FET model is used in Section III to compare the power-added efficiencies obtained with such signals when the amplifier is operating in the proposed class-Ã mode, and in the classical class-A and class-B modes. In Section IV, a more realistic FET model is employed, which is still simple enough to facilitate closed-form analysis. Effects due to nonlinearities in the gate and drain circuits, drain-to-gate feedback, and parasitic and load reactances, which would adversely affect all three classes of operation, are neglected.

II. Signal Statistics

Let the input voltage to the FET amplifier assume the general form

$$v_i(t) = V_i(t)\cos[\omega t + \phi(t)] \tag{1}$$

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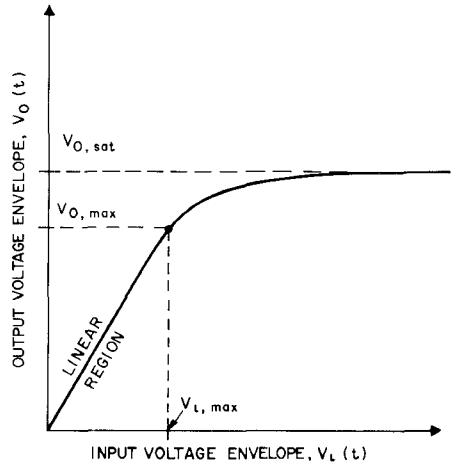

Fig. 2. Typical input–output RF envelope characteristic of an FET power amplifier

where $V_i(t)$ is the time-varying input envelope. Assuming that amplitude-to-phase (AM/PM) conversion is negligible, or has been compensated for, one can write the corresponding output voltage as

$$v_o(t) = V_o(t)\cos[\omega t + \phi(t)] \tag{2}$$

where $V_o(t)$ is the time-varying output envelope. Both $V_i(t)$ and $V_o(t)$ are defined to be nonnegative quantities.

A typical input–output envelope characteristic of an FET amplifier consists of an essentially linear region followed by a sharply saturating region as shown in Fig. 2. The maximum input and output voltages of the *linear* region are denoted by $V_{i,\max}$ and $V_{o,\max}$, respectively, and the output saturation voltage by $V_{o,\text{sat}}$. In practice, $V_{i,\max}$ and $V_{o,\max}$ may be defined at, say, the 1-dB output compression point. Typically, $V_{o,\text{sat}}$ exceeds $V_{o,\max}$ by up to about two decibels.

Define the normalized output envelope as

$$r(t) = V_o(t)/V_{o,\max}. \tag{3}$$

The efficiency computations given in the next two sections require the knowledge of the mean ($\bar{r}$) and mean-square ($\overline{r^2}$) values of $r(t)$. Some of these values are given in Table I for various signaling schemes. In all cases, with the exception of case 3, the signal envelope is assumed to lie entirely within the linear range, with $\max[r(t)] = 1$. Rectangular pulses were assumed in the computations for the cases involving digitally modulated signals.

In case 3, the input signal is essentially Gaussian, and hence its envelope has a Rayleigh distribution [7], which, theoretically, goes to infinity. Thus the amplifier drive level can be best described by its output power backoff, which, for the purpose of this paper, is defined as (cf. [8], [9])

$$B_o = \frac{\text{maximum single-carrier linear output power}}{\text{average multicarrier output power}}$$

$$= V_{o,\max}^2 / \overline{V_o^2(t)} = 1/\overline{r^2} \tag{4}$$

which results in the value of $\overline{r^2}$ shown in Table I. The corresponding value of $\bar{r}$ is obtained by assuming that $r(t)$, like the input envelope, has a Rayleigh distribution, and hence [10], $\bar{r} = (\pi \overline{r^2}/4)^{1/2}$. This assumption is, of course, only true if the amplifier is strictly linear. However, the resulting error would be negligible under normal multicarrier operating conditions where B_o is more than a few decibels.

TABLE I
MEAN AND MEAN-SQUARE VALUES OF THE NORMALIZED OUTPUT ENVELOPE $r(t)$ FOR VARIOUS SIGNALING SCHEMES

Case	Signaling Scheme	$\overline{r^2}$	$\bar{r}$
1	One PM or FM Carrier	1	1
2	Two Equal-Power PM or FM Carriers	0 5	0 637
3	Large Number of PM or FM Carriers (Also SSB and Gaussian Signals)	$\frac{1}{B_o}$	$\frac{1}{2}\sqrt{\frac{\pi}{B_o}}$
4	16-QAM (4×4 Square Array)	0 556	0 706
5	64-QAM (8×8 Square Array)	0 429	0.615
6	256-QAM (16×16 Square Array)	0 378	0 576
7	Infinitely Packed Square Array	0 333	0 541
8	Infinitely Packed Disc	0 5	0 667

III. EFFICIENCIES FOR AN IDEALIZED FET MODEL

A. The Three Classes of Operation

An idealized FET model is shown in Fig. 3 together with its gate-voltage v_G, drain-current i_D, and drain-voltage v_D characteristics. In Fig. 3, V_p is the gate pinch off voltage, V_m is the maximum allowable drain voltage, and I_m is the maximum drain current, which is obtained at zero gate voltage. (Actually, a slightly larger drain current can be obtained if the gate voltage is permitted to be positive.)

As shown in the figure, the gate dc bias voltage E_G that is required to operate the FET in standard class A, the newly proposed class Ã (as depicted in Fig. 1), or standard class B is given, respectively, by

$$E_G^A = -V_p/2 \tag{5a}$$

$$E_G^{\tilde{A}}(t) = -V_p + V_i(t) \tag{5b}$$

$$E_G^B = -V_p \tag{5c}$$

where $V_i(t)$ is the input RF voltage envelope, which is a nonnegative quantity as mentioned in Section II. If $V_i(t) \geq V_p/2$, then $E_G^{\tilde{A}}$ is set to $-V_p/2$. The drain dc bias voltage E_D, and the RF load resistance (R_L), which are identical for the three classes, are given by

$$E_D = V_m/2 \tag{6}$$

$$R_L = V_m/I_m. \tag{7}$$

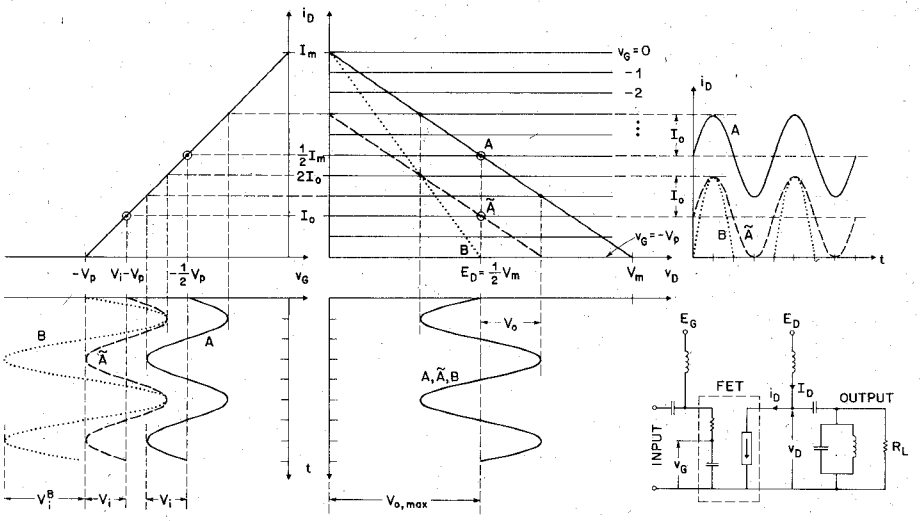

Fig. 3. An idealized FET model showing the load lines, and the voltage and current waveforms for operation in class A (solid lines), class $\tilde{A}$ (dashed lines), and class B (dotted lines).

The resistive load lines, and the voltage and current waveforms for classes A, $\tilde{A}$, and B, are shown in Fig. 3 by solid, dashed, and dotted lines, respectively. The slopes of each of the load lines for classes A and $\tilde{A}$ is $-1/R_L$ while that for class B is $-2/R_L$. The load line for class $\tilde{A}$ moves up and down parallel to itself in response to gate bias voltage variations. The other two load lines remain fixed. The relative magnitudes of the various waveforms for the three classes are chosen in Fig. 3 to yield the same output RF voltage envelope $V_o(t)$ and hence, the same output power, since the load resistances of the three classes are identical.

The drain current for class B is a half-wave rectified sinusoid. Thus a parallel tuned circuit is needed in the output to filter out the harmonics. Actually, since these harmonics are all even, a short-circuited quarter-wave transmission line may be employed instead. The use of two FET's in a push–pull mode would eliminate the need for an output filter. This mode of operation, however, is not easily realizable at microwave frequencies.

B. Power and Efficiency Computations

The RF output power, which is time dependent because of signal envelope variations, is given by

$$P_o(t) = V_o(t) I_o(t)/2 \tag{8}$$

where $I_o(t) = V_o(t)/R_L$ is the fundamental-frequency component of $i_D(t)$. Noting from Fig. 3 that $V_{o,\max} = V_m/2$, and employing (3) and (7), one obtains for any of the three classes

$$P_o(t) = r^2(t) V_m I_m/8. \tag{9}$$

The dc drain power, which is also time dependent, is given by

$$P_D(t) \equiv E_D I_D(t) \tag{10}$$

where $I_D(t)$ is the dc component of $i_D(t)$. It follows from the current waveforms of Fig. 3 that

$$P_D^{A} = V_m I_m/4 \tag{11a}$$

$$P_D^{\tilde{A}}(t) = r(t) V_m I_m/4 \tag{11b}$$

$$P_D^{B}(t) = r(t) V_m I_m/2\pi. \tag{11c}$$

The *drain* efficiency is defined by

$$\eta_D \equiv \bar{P}_o/\bar{P}_D \tag{12}$$

where the overbars indicate averaging over signal envelope variations, i.e., over $r(t)$. Thus (9), (11), and (12) give

$$\eta_D^{A} = \overline{r^2}/2 \tag{13a}$$

$$\eta_D^{\tilde{A}} = \overline{r^2}/2\bar{r} \tag{13b}$$

$$\eta_D^{B} = \pi\, \overline{r^2}/4\bar{r}. \tag{13c}$$

Note that for a fully driven constant-envelope signal, where $\bar{r} = \overline{r^2} = 1$ (case 1 in Table I), the drain efficiencies of class A (or $\tilde{A}$) and class B attain their classical values of 50 and 78.5 percent, respectively. The corresponding efficiencies for varying-envelope signals (remaining cases in Table I) are significantly smaller than these values.

The *power-added* efficiency, which is the main quantity of interest, is defined by

$$\eta_{\text{added}} = (\bar{P}_o - \bar{P}_i)/\bar{P}_D \tag{14a}$$

$$= \eta_D(1 - 1/G) \tag{14b}$$

where $\bar{P}_i$ is the average input RF power, and G is the power gain defined by

$$G = \bar{P}_o/\bar{P}_i. \tag{15}$$

If the gate capacitance of the FET is assumed to be linear, it follows that $\bar{P}_i$ is proportional to $\overline{V_i^2}$. It is noted from Fig. 3 that, for the same output power, V_i for class $\tilde{A}$ has the same value as that for class A, while that for class B has twice that value. Thus the power gain of the three

classes are related by

$$G_{\tilde{A}} = G_A \tag{16a}$$

$$G_B = G_A/4. \tag{16b}$$

Hence, for a given FET, class-B gain is 6 dB less than that of either class A or $\tilde{A}$. This prevents class-B operation at higher microwave frequencies [11] where currently available high-power FET's have class-A linear gains in the vicinity of 6 dB.

It is appropriate to mention at this point that the above computations are made under the assumption that the maximum allowable drain voltage V_m is the same for classes A, $\tilde{A}$, and B. Actually, the fundamental quantity to be limited is the maximum gate-to-drain voltage swing $V_{GD,\max}$ [11]. Thus since the maximum negative gate voltage swing is $-2V_p$ for class B, and only $-V_p$ for class A or $\tilde{A}$, it follows that $V_m^A = V_m^{\tilde{A}} = V_{GD,\max} - V_p$, while $V_m^B = V_{GD,\max} - 2V_p$. Hence the maximum output RF power for class B is less than that for class A or $\tilde{A}$ by an amount equal to $V_p I_m/8$. Of course, this reduction in power causes class-B gain to suffer an additional reduction beyond that given in (16b).

C. Comparison of Efficiencies

It follows from (13), (14), and (16) that, for a given FET with an associated class-A gain of G_A, the power-added efficiencies of the three classes of operation are related by

$$\eta_{\text{added}}^{\tilde{A}} / \eta_{\text{added}}^{A} = 1/\bar{r} \tag{17a}$$

$$\eta_{\text{added}}^{B} / \eta_{\text{added}}^{\tilde{A}} = \frac{\pi}{2} \frac{G_A - 4}{G_A - 1} \tag{17b}$$

$$\eta_{\text{added}}^{B} / \eta_{\text{added}}^{A} = \frac{\pi}{2\bar{r}} \frac{G_A - 4}{G_A - 1}. \tag{17c}$$

Table I and (17a) indicate that, depending on the signaling scheme, the power-added efficiency of class $\tilde{A}$ is significantly superior (by a factor of 1.4 to 2.2) to that of class A. These two classes are, of course, identical for a fully driven constant-envelope signal (case 1 in Table I). It follows from (17b) and (17c) that, because of the higher drain efficiency of class B, its power-added efficiency is greater than that of either class A or $\tilde{A}$ *if* the FET power gain is sufficiently high. However, it is evident from (17b) that if G_A is less than $4 + 6/(\pi - 2)$ (i.e., 9.7 dB), which is the usual case for higher microwave frequencies, then class $\tilde{A}$ has the highest efficiency.

The power-added efficiencies of the three classes of operation are plotted in Fig. 4 as a function of the power gain for a multicarrier signal (case 3 in Table I) with an output power backoff B_o of 4 dB. If $V_{o,\text{sat}} \approx V_{o,\max}$ in the envelope characteristic of Fig. 2, and if AM/PM conversion is neglected, it is shown in [8] and [9] that this value of backoff yields a carrier-to-intermodulation ratio of about 20 dB.

Fig. 4 also shows the power-added efficiencies of classes A (or $\tilde{A}$) and B with a fully driven constant-envelope signal (case 1 in Table I). Interestingly, it can be shown that these efficiencies can be obtained for any varying-envelope signal, with classes $\tilde{A}$ and B, respectively, if the *drain* dc bias voltage is also dynamically controlled such that $E_D(t) = V_o(t)$. Dynamically varying the drain bias voltage, however, seems difficult because, unlike the gate, the drain draws a large dc current.

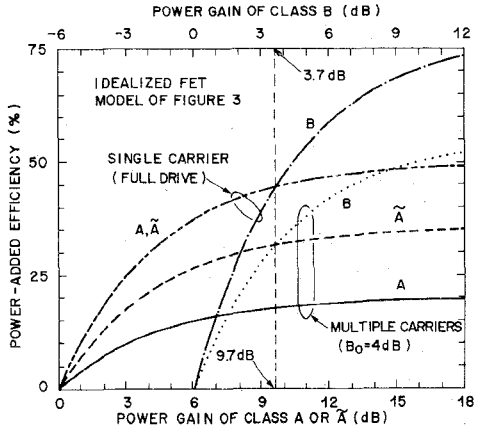

Fig. 4. Comparison of the power-added efficiency of the various classes of operation of the idealized FET model of Fig. 3 for a multicarrier signal (case 3 in Table I) with 4 dB of output backoff, and for a fully driven constant-envelope signal (case 1 in Table I). Note that operating the FET in class B results in a 6-dB reduction in gain compared to class A or $\tilde{A}$.

IV. Efficiencies for a More Realistic FET Model

We now consider the more realistic FET model shown in Fig. 5. In that model, the FET characteristics are described by the three basic parameters, V_p, I_m, and V_m, of the previous model, and by the three new dimensionless parameters, Δ, ϵ, and δ. As shown in the figure, the latter parameters account for the following three realistic features: 1) The $i_D - v_D$ characteristic for $v_G = 0$ has a knee at $i_D = I_m$, $v_D = \Delta V_m$. 2) A constant drain conductance, $G_D = \epsilon I_m/V_m$, exists in the region $v_D \geq \Delta V_m$; thus the drain characteristic in that region is described by $i_D = j_D + G_D v_D$, where j_D is the drain current generator output, which is a function of v_G. 3) The $v_G - j_D$ characteristic is assumed to be linear only over the range from $v_G = 0$ down to $v_G = -(1-\delta)V_p$. It is noted that if $\Delta = \epsilon = \delta = 0$, then the model of Fig. 5 reduces to that of Fig. 3.

The bias and load conditions for operating in classes A, $\tilde{A}$, and B are

$$E_G^A = -V_p(1-\delta)/2 \tag{18a}$$

$$E_G^{\tilde{A}}(t) = -V_p(1-\delta) + V_i(t) \tag{18b}$$

$$E_G^B = -V_p. \tag{18c}$$

$$E_D = V_m(1+\Delta)/2 \tag{19}$$

$$R_L^A = R_L^{\tilde{A}} = \frac{V_m}{I_m} \frac{1-\Delta}{1-\epsilon-\delta+\Delta\epsilon\delta} \tag{20a}$$

$$R_L^B = V_m(1-\Delta)/I_m(1-\epsilon). \tag{20b}$$

The seemingly peculiar shape of the class-B load line in Fig. 5 results from the fact that the drain current is nonsinusoidal while the drain voltage is restricted to be

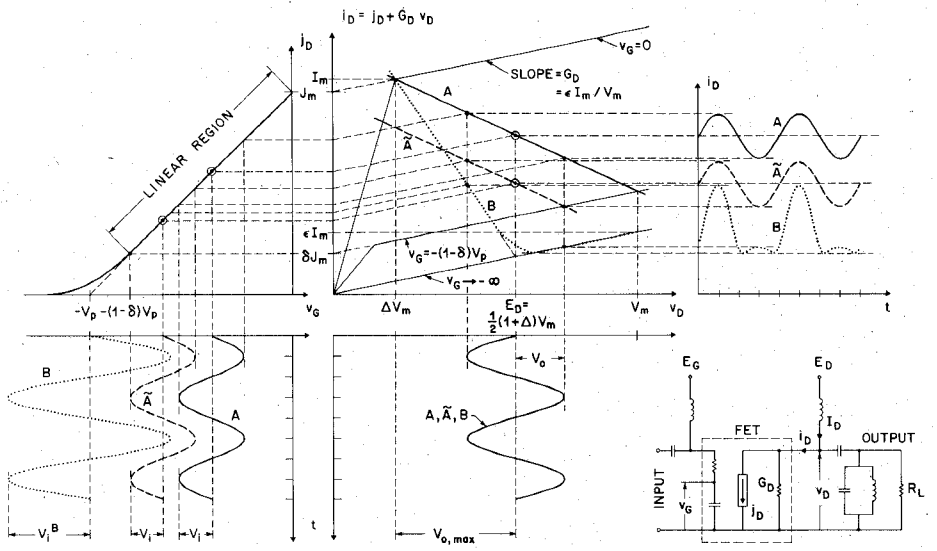

Fig. 5. A more realistic FET model, which is described by three dimensionless ideality parameters, Δ, ϵ, and δ, defined in Section IV. Note the difference in load lines and waveforms compared to the idealized model in Fig. 3. The two models become identical if $\Delta = \epsilon = \delta = 0$.

sinusoidal by the output tuned circuit. The relative magnitudes of the various waveforms for the three classes are chosen in the figure to yield the same $V_o(t)$, and hence, the same $r(t)$. However, the corresponding output power for class B differs from that for class A or Ã because of the difference in load resistances indicated in (20).

Following the same steps used in the previous section, it can be shown that the drain efficiencies of the three classes are

$$\eta_D^{\mathrm{A}} = \frac{\overline{r^2}}{2} \cdot \frac{1-\Delta}{1+\Delta} \cdot \frac{1-\epsilon-\delta+\Delta\epsilon\delta}{1+\epsilon+\delta-\Delta\epsilon\delta} \tag{21a}$$

$$\eta_D^{\tilde{\mathrm{A}}} = \frac{\overline{r^2}}{2} \cdot \frac{1-\Delta}{1+\Delta} \cdot \frac{1-\epsilon-\delta+\Delta\epsilon\delta}{[\bar{r}(1-\delta)+2\delta](1-\Delta\epsilon)+\epsilon(1+\Delta)} \tag{21b}$$

$$\eta_D^{\mathrm{B}} \approx \frac{\pi\overline{r^2}}{4} \cdot \frac{1-\Delta}{1+\Delta} \cdot \frac{1-\epsilon}{\bar{r}(1-\Delta\epsilon)+\pi\epsilon(1+\Delta)/2}. \tag{21c}$$

It can also be shown that the power gains of the three classes are related by

$$G_{\tilde{\mathrm{A}}} = G_{\mathrm{A}} \tag{22a}$$

$$G_{\mathrm{B}} = \frac{G_{\mathrm{A}}}{4} \cdot \frac{(1-\epsilon)(1-\delta)^2}{1-\epsilon-\delta+\Delta\epsilon\delta}. \tag{22b}$$

Note that the difference in gains between classes A and B is no longer exactly 6 dB.

The power-added efficiencies of the three classes of operation can now be computed and compared through the use of (14), (21), and (22). For example, with $\Delta = \epsilon = \delta = 0.05$, these efficiencies are plotted in Fig. 6 as a function of the power gain for a multicarrier signal (case 3 in Table I) with an output backoff B_o of 4 dB. The power-added efficiencies of classes A (or Ã) and B with a fully driven constant-envelope signal (case 1 in Table I) are also plotted in Fig. 6. Although the efficiency values in this figure are

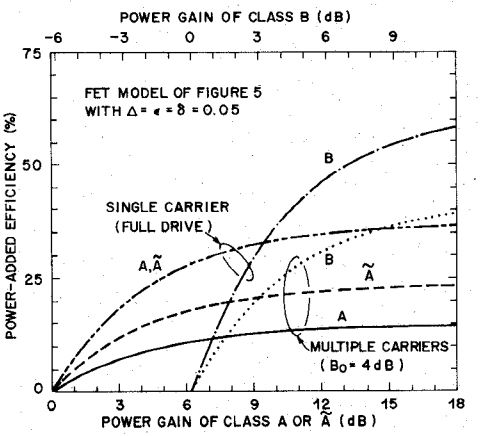

Fig. 6. Comparison of the power-added efficiency of the various classes of operation for the more realistic FET model of Fig. 5 with $\Delta = \epsilon = \delta = 0.05$. Note that the gain reduction for class-B operation is slightly more than 6 dB.

less than the corresponding values given in Fig. 4 for the idealized FET model, their interrelations remain essentially unchanged.

It is appropriate to mention at this point that the computations given in this section for classes A and Ã are based on the model with no further assumptions or approximations. However, in computing the class-B fundamental frequency component of the drain current, which is needed in (20b), (21c), and (22b), it was assumed that, in the nonlinear region of the $j_D - v_G$ characteristic, the difference between j_D for $\delta \neq 0$ and that for $\delta = 0$ is an even function of $v_G + V_p$. Under this assumption the harmonics of $i_D(t)$ would be all even, the amplifier would be linear, and (20b) and (22b) would be exact. However, in computing the dc component of $i_D(t)$, which is needed in (21c), the effect of the $j_D - v_G$ nonlinearity was neglected to avoid unnecessary complexity. Exact computations would have resulted in a small positive quantity, on the order of δ^2, to be added to the denominator of the last fraction in (21c).

V. Discussions and Conclusions

When operating with varying-envelope signals, a linear class-A FET power amplifier has low drain efficiency, and, hence, also low power-added efficiency. Class-B operation offers significantly higher drain efficiency, but at a large cost in power gain (about 6 dB less gain than that of class A using the same device). Thus a high power-added efficiency can be obtained from class B only when the gain is high (more than about 10 dB for class A, i.e., 4 dB for class B). Hence, class B is only suitable at lower microwave frequencies, where such high gains are available.

The proposed class-Ã operation depicted in Fig. 1 has the same gain as class A, and a drain efficiency that is almost as high as that of class B. As shown in Figs. 4 and 6, it yields a power-added efficiency that is more than 50 percent larger than that of class A, independently of the gain. The efficiency is also better than that of class B, if the gain is moderate or low (less than about 10 dB for class A or Ã). Thus class Ã provides a significant increase in efficiency at higher microwave frequencies where only moderate or low power gains are currently available.

As mentioned in the Introduction, linear operation of class Ã requires the $i_D - v_G$ transfer characteristic of the FET to be essentially linear over most of its operating range, which is possible if the FET has a specially shaped channel-doping profile [1]–[4]. This, of course, may not be true for some FET's. In fact, it was suggested in [12] to use gate-bias control, whose polarity is opposite to that of class Ã, to improve the FET linearity. However, in such cases, linear class-Ã operation is still possible through the use of a predistortion linearizer [8], [9] to compensate for the resulting nonlinear distortion. The detected envelope voltage of the signal, which is needed in class-Ã operation, can also be used to control a varactor phase shifter, inserted before the amplifier, to compensate for the AM/PM nonlinearity of the FET [13].

In conclusion, class Ã is a promising mode of operation for FET amplifiers operating with varying-envelope signals. Its potentially higher efficiency should justify the added circuit complexity, and the possibly more stringent requirement on the shape of the channel-doping profile of the FET.

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